IN THE CLAIMS:

Please cancel claims 10-11 without prejudice, amend claim 1 and accept new claims 12-20 as follows:

1. (currently amended) A thin film transistor array panel comprising:

first and second gate members connected to each other;

a gate insulating layer formed on the first and the second gate members;

first and second semiconductor members formed on the gate insulating layer ~~opposite the first and the second gate members~~, respectively;

first and second source members connected to each other and located near the first and the second semiconductor members, respectively;

first and second drain members located near the first and the second semiconductor members, respectively, and located opposite the first and the second source members ~~with respect to the first and the second gate members~~, respectively; and

a pixel electrode connected to the first and the second drain members,

wherein the first gate member, the first semiconductor member, the first source member, and the first drain members form a first thin film transistor, and the second gate member, the second semiconductor member, the second source member, and the second drain members form a second thin film transistor.

2. (original) The thin film transistor array panel of claim 1, wherein the first thin film transistor and the second thin film transistor are symmetrically aligned.

3. (original) The thin film transistor array panel of claim 2, wherein the alignment of the first and the second thin film transistors are symmetrical with respect to a predetermined line.

4. (original) The thin film transistor array panel of claim 3, wherein the predetermined line includes a boundary line between shots in light exposure.

5. (original) The thin film transistor array panel of claim 4, further comprising a third thin film transistor different from the first and the second thin film transistors.

6. (original) The thin film transistor array panel of claim 1, wherein the alignment of the first and the second thin film transistors are located opposite each other with respect to a boundary line between shots in light exposure.

7. (original) The thin film transistor array panel of claim 1, wherein channels of the first and the second thin film transistors have curved shapes.

8. (original) The thin film transistor array panel of claim 7, wherein channels of the first and the second thin film transistors have U or C shapes.

9. (original) The thin film transistor array panel of claim 1, wherein the first and the second semiconductor members have substantially the same planar shapes as the

first and the second source and drain members except for channel portions of the first and the second thin film transistors.

10 – 11. (canceled)

12. (new) A thin film transistor array panel comprising:

first and second gate members connected to each other;

a gate insulating layer formed on the first and the second gate members;

first and second semiconductor members formed on the gate insulating layer;

first and second source members connected to each other and located over the first and the second semiconductor members, respectively;

first and second drain members located over the first and the second semiconductor members, respectively, and located opposite the first and the second source members, respectively; and

a pixel electrode connected to the first and the second drain members,

wherein the first gate member, the first semiconductor member, the first source member, and the first drain members form a first thin film transistor, and the second gate member, the second semiconductor member, the second source member, and the second drain members form a second thin film transistor.

13. (new) The thin film transistor array panel of claim 12, wherein the first thin film transistor and the second thin film transistor are symmetrically aligned.

14. (new) The thin film transistor array panel of claim 13, wherein the alignment of the first and the second thin film transistors are symmetrical with respect to a predetermined line.

15. (new) The thin film transistor array panel of claim 14, wherein the predetermined line includes a boundary line between shots in light exposure.

16. (new) The thin film transistor array panel of claim 15, further comprising a third thin film transistor different from the first and the second thin film transistors.

17. (new) The thin film transistor array panel of claim 12, wherein the alignment of the first and the second thin film transistors are located opposite each other with respect to a boundary line between shots in light exposure.

18. (new) The thin film transistor array panel of claim 12, wherein channels of the first and the second thin film transistors have curved shapes.

19. (new) The thin film transistor array panel of claim 18, wherein channels of the first and the second thin film transistors have U or C shapes.

20. (new) The thin film transistor array panel of claim 12, wherein the first and the second semiconductor members have substantially the same planar shapes as the first

and the second source and drain members except for channel portions of the first and the second thin film transistors.